Kentron Technologies- Introducing QBM™ (Quad Band Memory) Technology

Robert J. Goodman, CEO

Badawi Dweik, Field Applications Manager

San Jose January 23-24, 2001 • Taipei February 14-15, 2001

Kentron Technologies

- Founded in 1996
- Corporate Headquarters:
  - Executive Staff
  - Sales, Marketing, and Finance
  - Engineering and R & D
  - Operations and Service
  - Finished goods inventory
- Additional Sales/Support offices

in San Jose, CA and Austin, TX

155 West Street, Wilmington, MA 01887, USA

Members Of:

Platform Conference

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Mission Statement

Provide Advanced Memory Platforms That Increase Bandwidth and Density for the Telecom and Internet Infrastructure.

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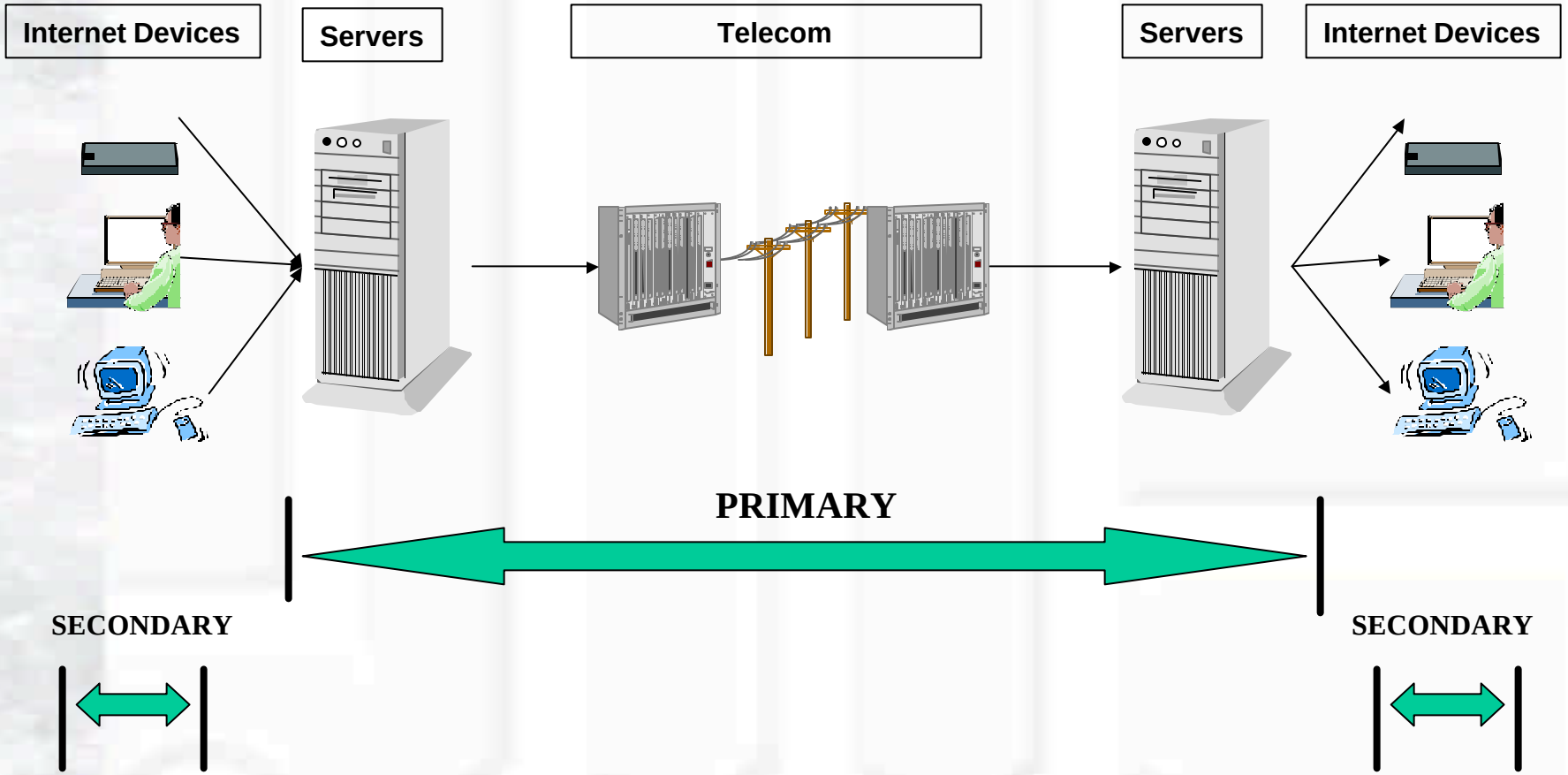
Advanced Memory Platforms For:



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Technology Offerings

Kentron's **Low Cost** Solutions Span the "Market Requirements" Spectrum

Density  ***Speed***

Low Profile Platform
Patent Pending Module Solutions for Notebooks and "1U" Server Platforms

FEMMA^{tm} Platform
Patented Module Solutions for Maximum Density Requirements

E-BUS^{tm} Platform
Patented Technology for Minimizing Loading Delays

QBM^{tm} Platform
Patent Pending Technology provides Highest Memory Bandwidth

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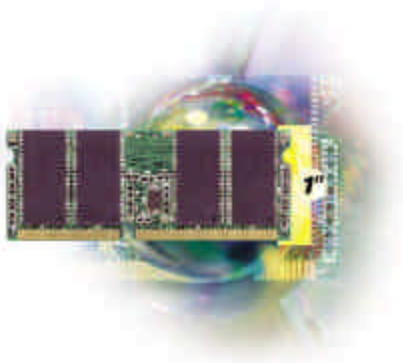
Kentron Low Profile Platform Solutions



- 1” Low Profile SODIMMs
  - ***PC200/PC266***/PC100/PC133
  - 32MB ~ 256MB (Single board)
  - **512MB** (FEMMA Platform, Q2, FY01) **NEW**

- 1.2” Low Profile DIMMS
  - ***PC200/PC266***/PC100/PC133
  - Registered or Buffered (ECC or non-ECC)
  - 128 MB ~ 512 MB
  - **“The GIG™”** (FEMMA Platform) **NEW**

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FEMMA™ Platform

***F**oldable **E**lectronic **M**emory **M**odule **A**ssembly*

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FEMMA^{tm} *Platform*

- **Reliable**-proven technology that operates at significantly cooler temperatures and lower costs than stacked solutions.
- **Available**-patented non-stacking FEMMA module packaging design.
- **Scalable**-excellent platform for **Double Data Rate, Sync Flash, FBGA** and other future chip technologies.

FEMMA^{tm} efficiently addresses the requirements for high memory density, low thermals and the need for low cost.

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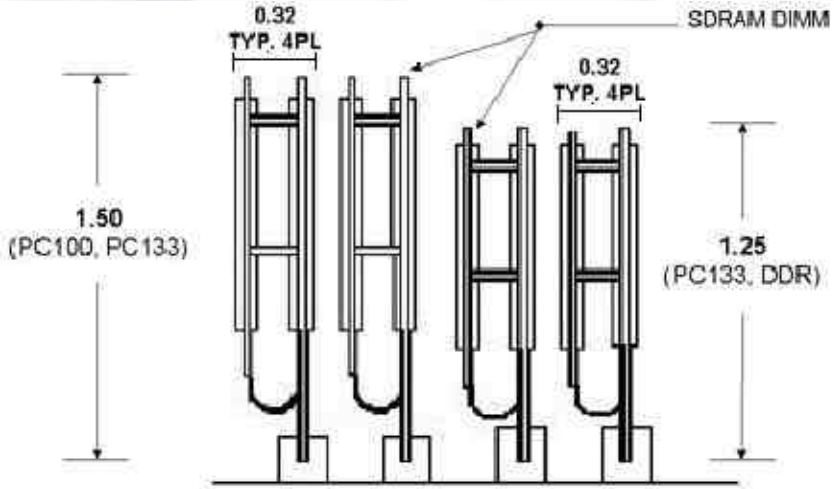
FEMMA™ *Platform*



Side View
Four Modules Mounted On Mother Board

- FEMMA fits into standard motherboard sockets.
- FEMMA possesses excellent reliability and thermal characteristics.*
- FEMMA is easily scalable to future chip technologies (FBGA, Sync Flash, etc.).
- FEMMA is low profile (1.25” & 1.50”).

Based on HALT and Harvard Thermal Testing results

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Module Time Line To Availability -Stacked vs. FEMMA™

Stacked Process (10 days to 2 weeks)

1. Memory sent to stacking company (2 days)	2. Memory stacked (3 to 5 days)	3. Stacked memory tested (1 day)	4. Memory sent back to Manufacturer (2 days)	5. Stacked memory placed on modules (1 to 2 days)	6. Stacked modules tested (1 day)

FEMMA™ (1 day)

1. Memory sent to module manufacturing line	2. Memory placed on FEMMA modules (same day)	3. FEMMA modules tested (same day)

TIME SAVED IS MONEY SAVED!

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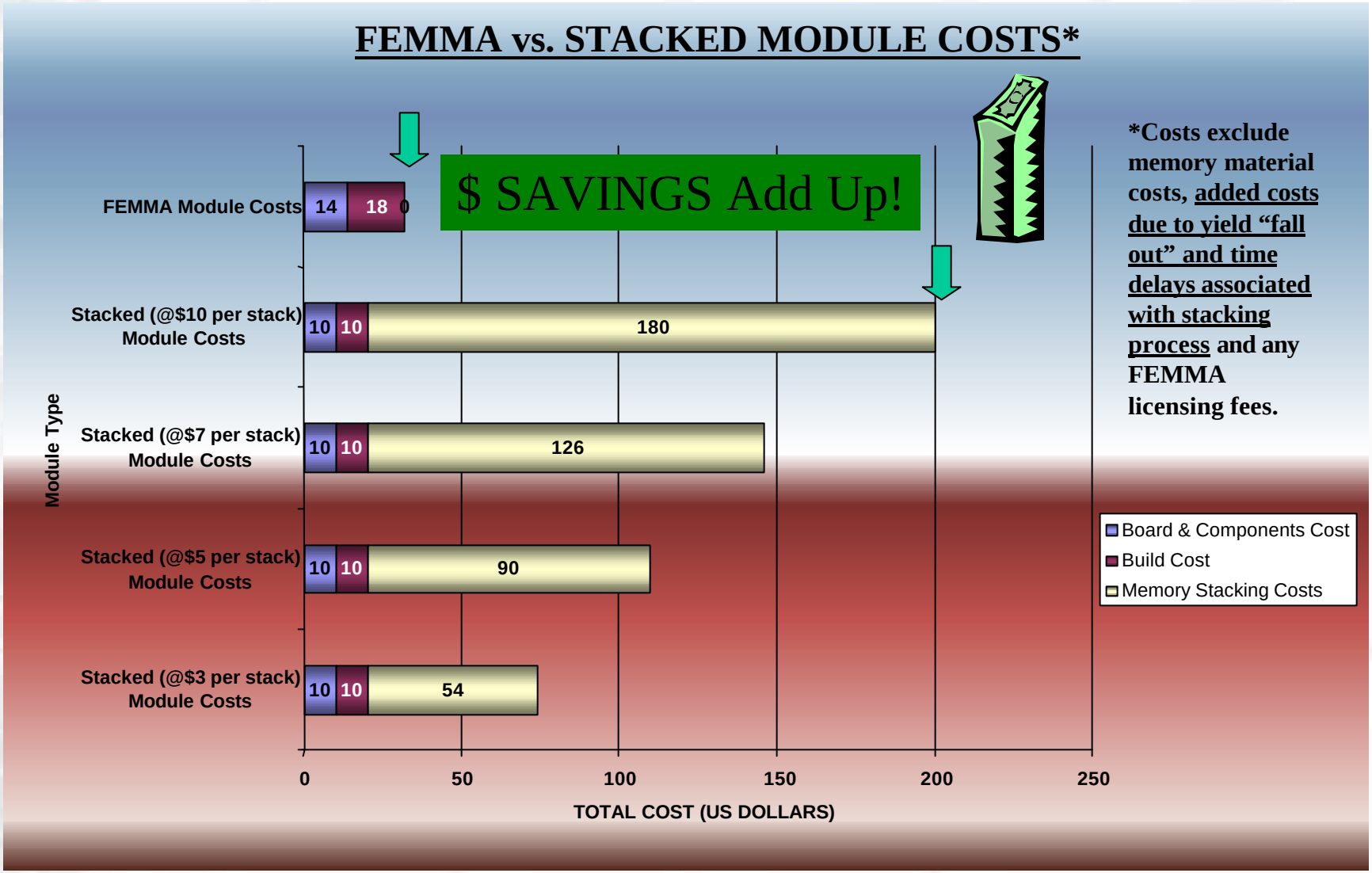
FEMMA vs. STACKED MODULE COSTS*



***Costs exclude memory material costs, <u>added costs due to yield "fall out" and time delays associated with stacking process</u> and any FEMMA licensing fees.**

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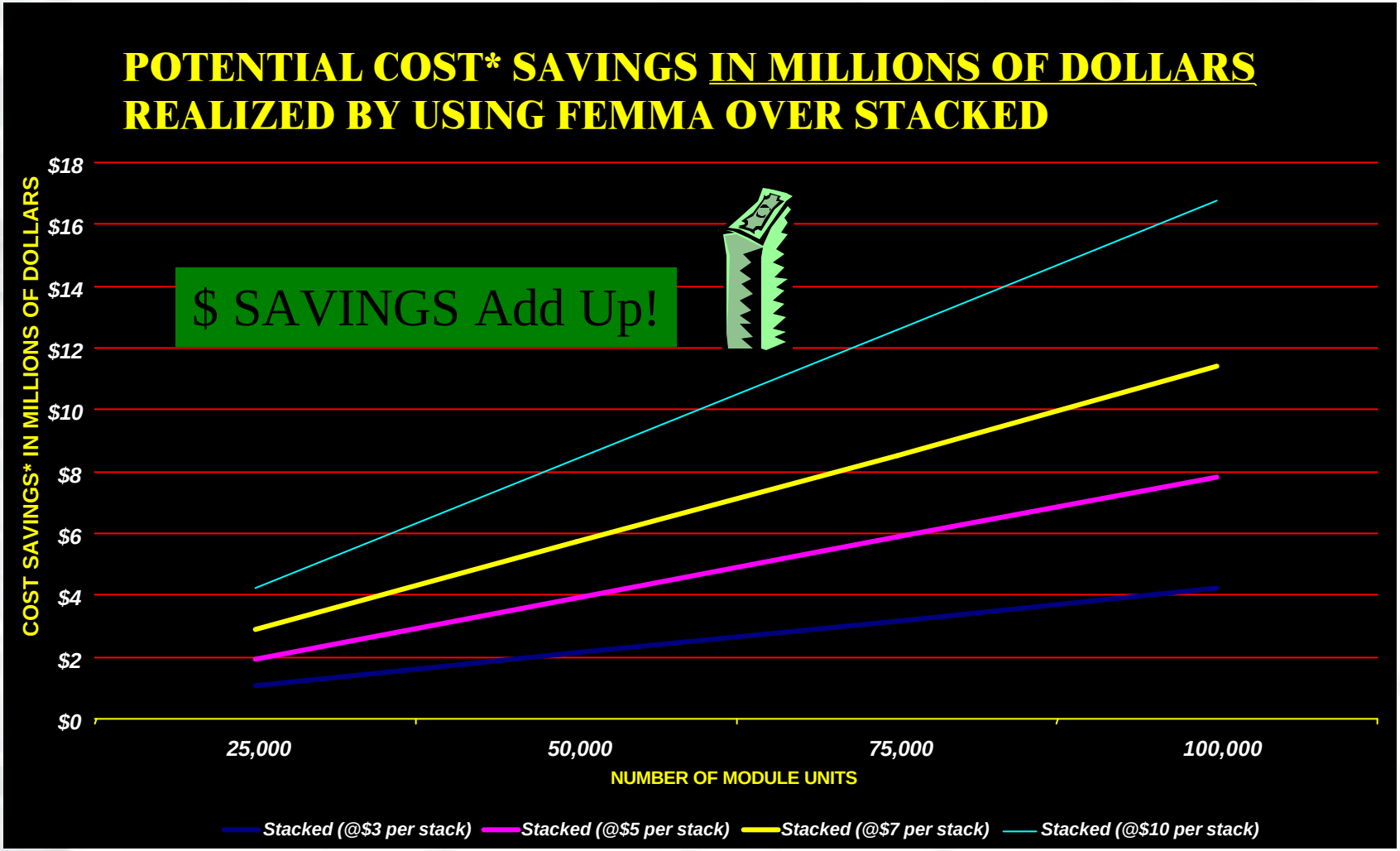

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ADVANCED MEMORY PLATFORM ROADMAP

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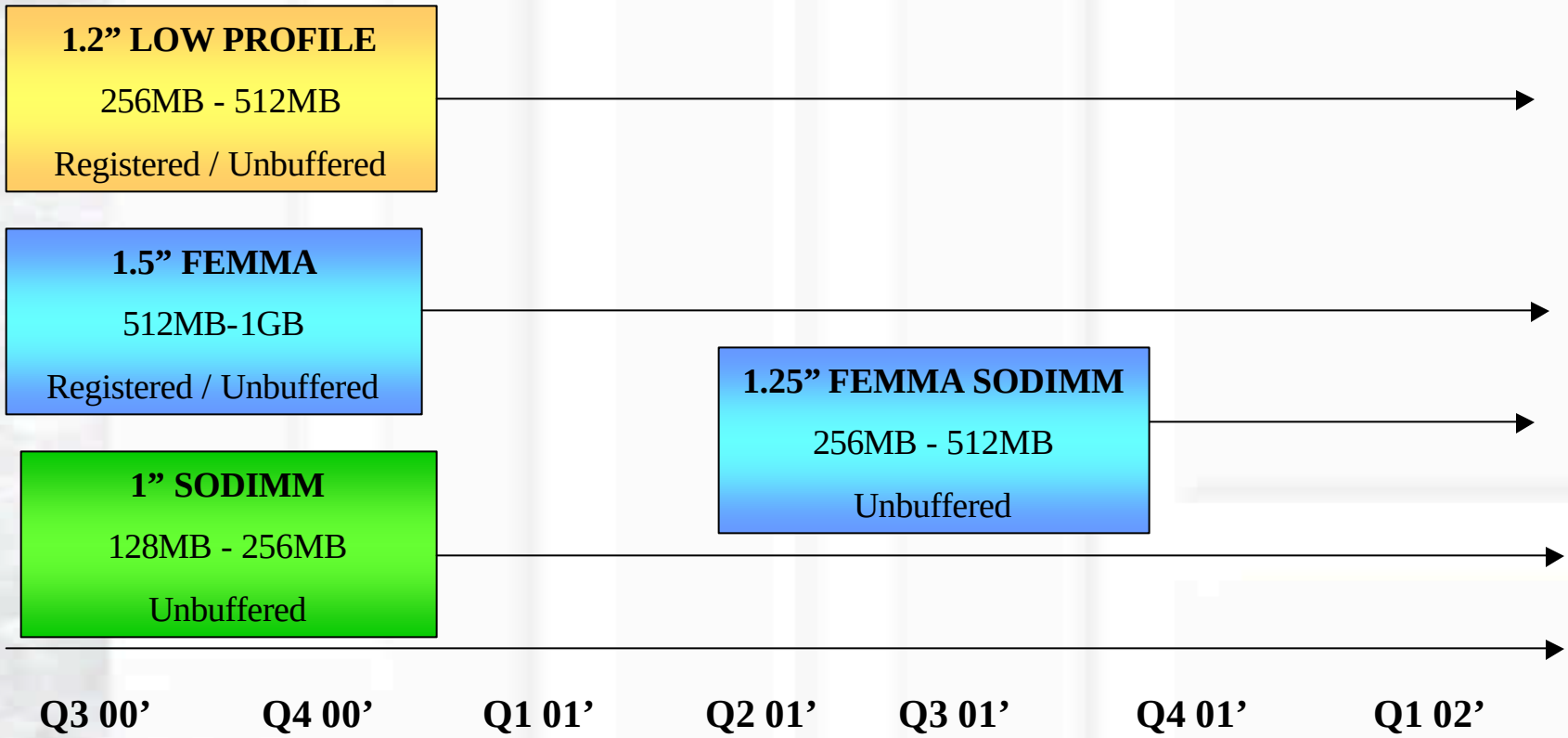
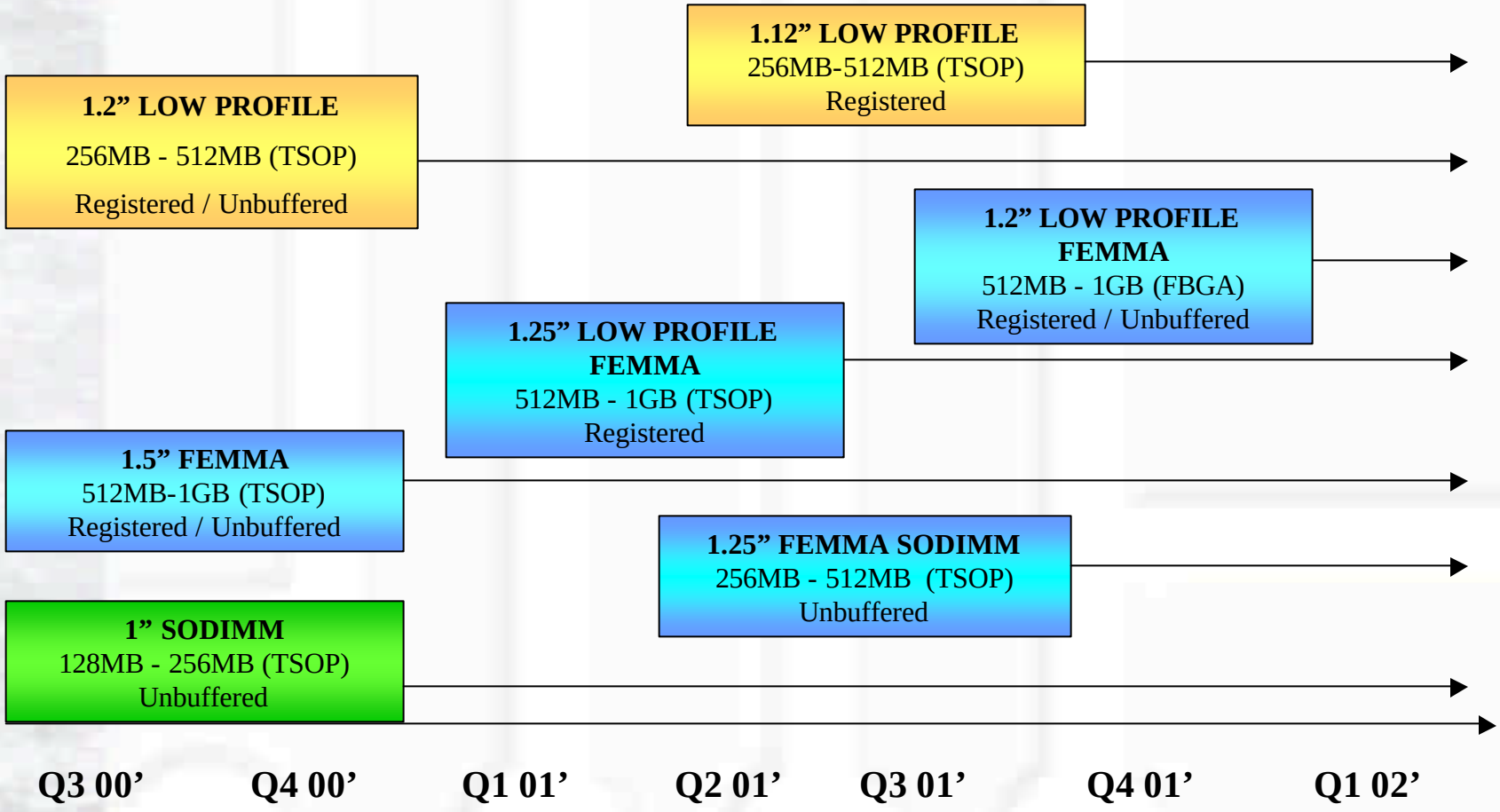
High Density PC100 Roadmap



High Density PC133 Roadmap



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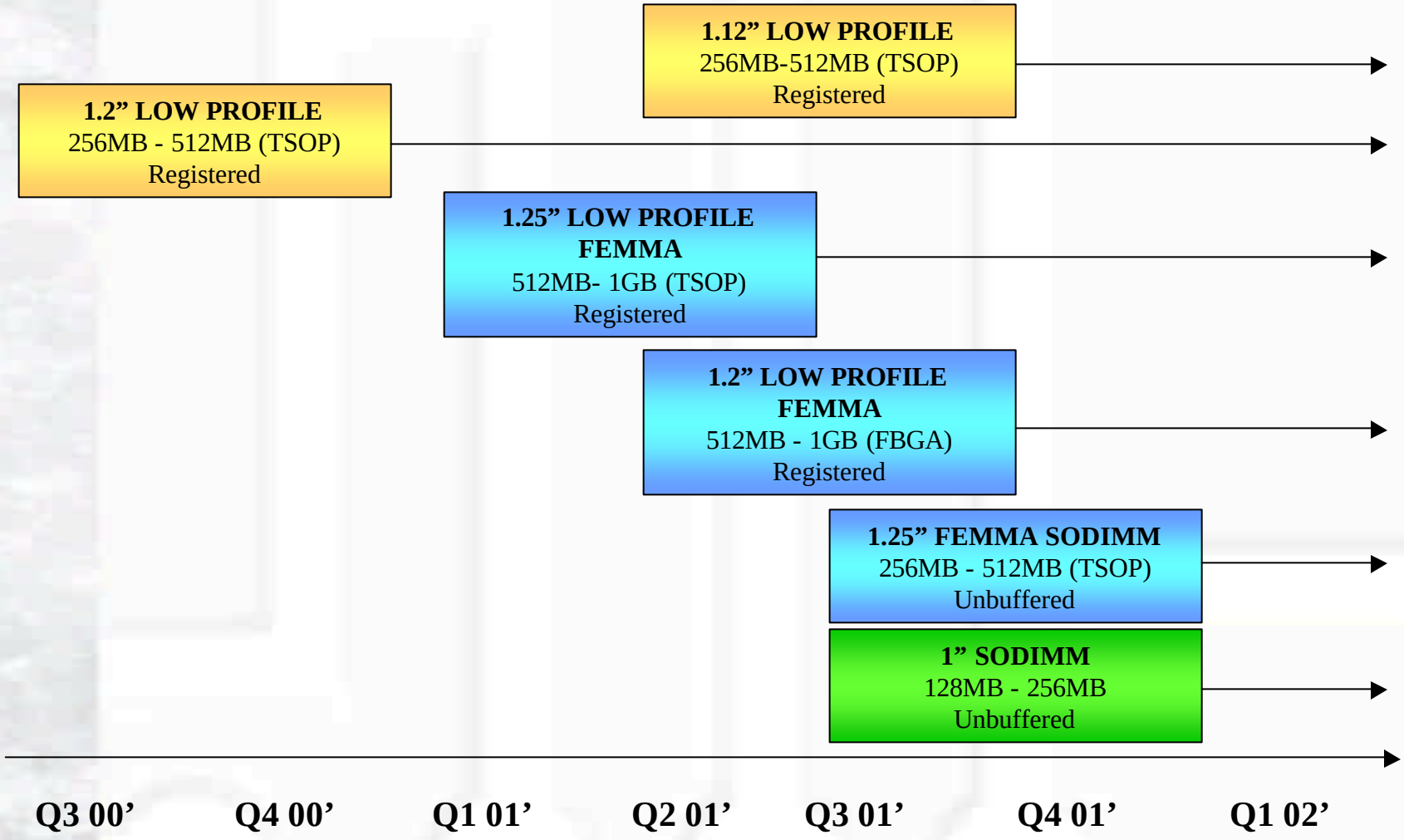
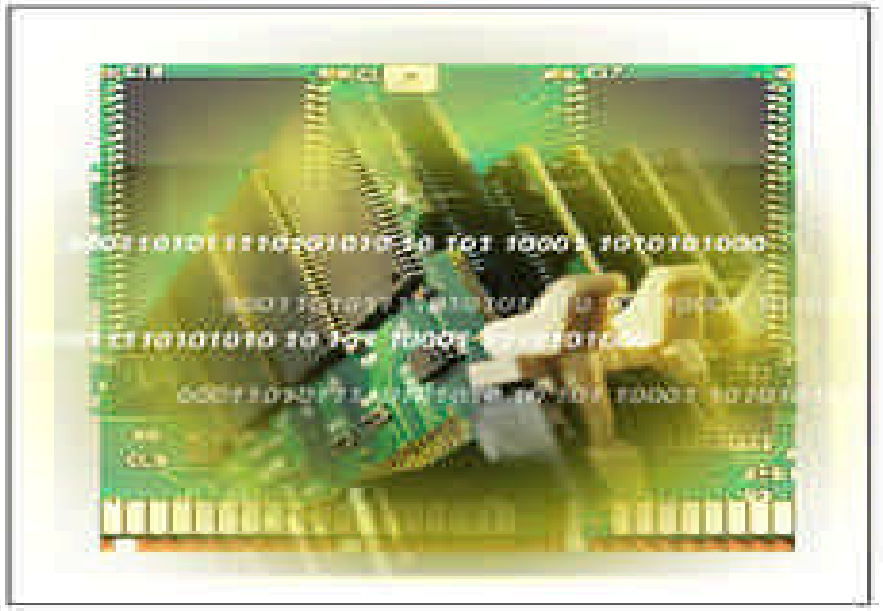
High Density DDR Roadmap



*E-BUS™ Technology**



***A method and apparatus for enhancing memory speed and capacity utilizing a set of electronic switches to isolate the computer data bus from the memory chips.**

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Excerpt from DDR Motherboard Errata Sheet

"When four DIMMs are installed the extra loading causes the system not meet specifications during some high activity transactions at 133MHz (PC2100). During these conditions the system will become ***unstable*** *causing* ***system lockup*** *or possible* ***data corruption****. As a result the board can only support a maximum of* ***three*** *double sided DIMMs when running at a 133MHz (PC2100). When running at 100MHz (PC1600) the system will support all four DIMM sockets populated with double sided DIMMs."*

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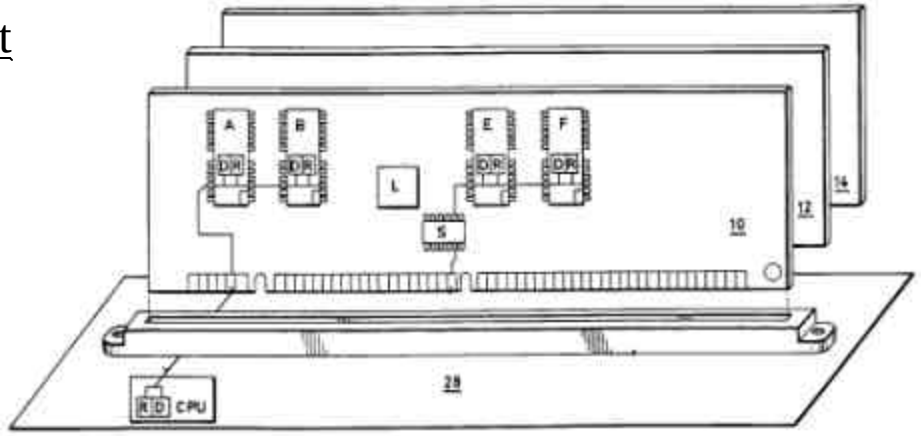
E-Bus Technology

- Server OEMs are limited by capacitive load issues from using faster memory and controlling larger amounts of data more efficiently in a memory bus system.
- The E-BUS technology provides significant competitive advantages:
  - Compliments the FEMMA solutions by minimizing the load presented to the system bus from multiple modules.
  - Ideal for MXT memory compression technologies.
- The patented E-Bus technology is the cornerstone of Kentron's QBM high bandwidth technology



QUAD BAND MEMORY (QBM™) TECHNOLOGY

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The need for *QBM*^{tm} is evident in the market

LETTERS

Speed Race Crashes Into Memory Wall

Your concern about the 1.5GHz clock rate in the Intel Willamette chip is only half the story ("Speed Race Moves into Fantasy Realm," Feb. 21, 2000, Page 8). The problem is not just the supporting wind tunnel, or the jumper wire problem. The major problem is that there is no memory, which is as far along as the 1.5GHz Willamette, which can keep up with the processor, so there will either have to be impossibly long pipelines or the machine will have a ton of wait-states to slow the effective clock down to nothing.

C. NORMAN WINNINGSTAD

"The major problem is that there is no memory, …which can keep up with the processor,…"

Electronic News -Viewpoint (May 1, 2000)

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Who suffers from these bottlenecks?

Servers

Telecom Equipment

Storage

Graphics, Video, HDTV

Portable

PCs, Workstations

DSPs, Wireless (Flash)

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QBM™ Technology

- Based on the principle that memory devices are never fast enough to meet bandwidth needs (and may never be fast enough).
- Provides the memory bandwidth of DDR 333 and DDR II (expected to be available in 2-5 years) to the industry **TODAY** using standard DDR I devices!
- A platform based technology that dramatically enhances the data transfer rate of standard, “off the shelf” SDRAM/DDR devices.
- Technology scalable to Sync FLASH, SSRAM, etc… or any device using Synchronous Data Transfer.
- E-BUS patent (use of FET switches to control SDRAM) is a cornerstone of the QBM technology.

HOW DOES QBM™ WORK?

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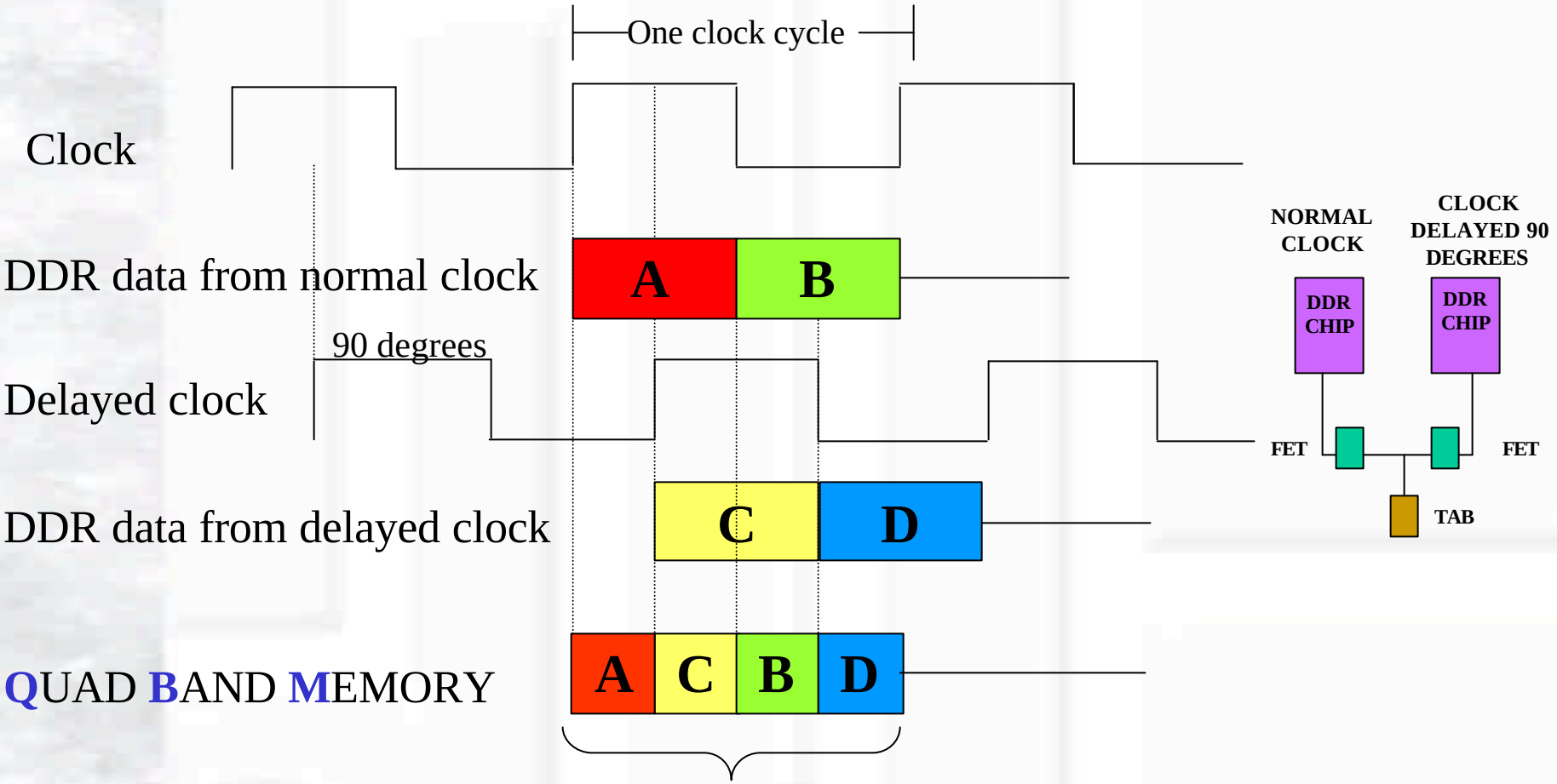
Quad Band Memory



4 times the bandwidth!

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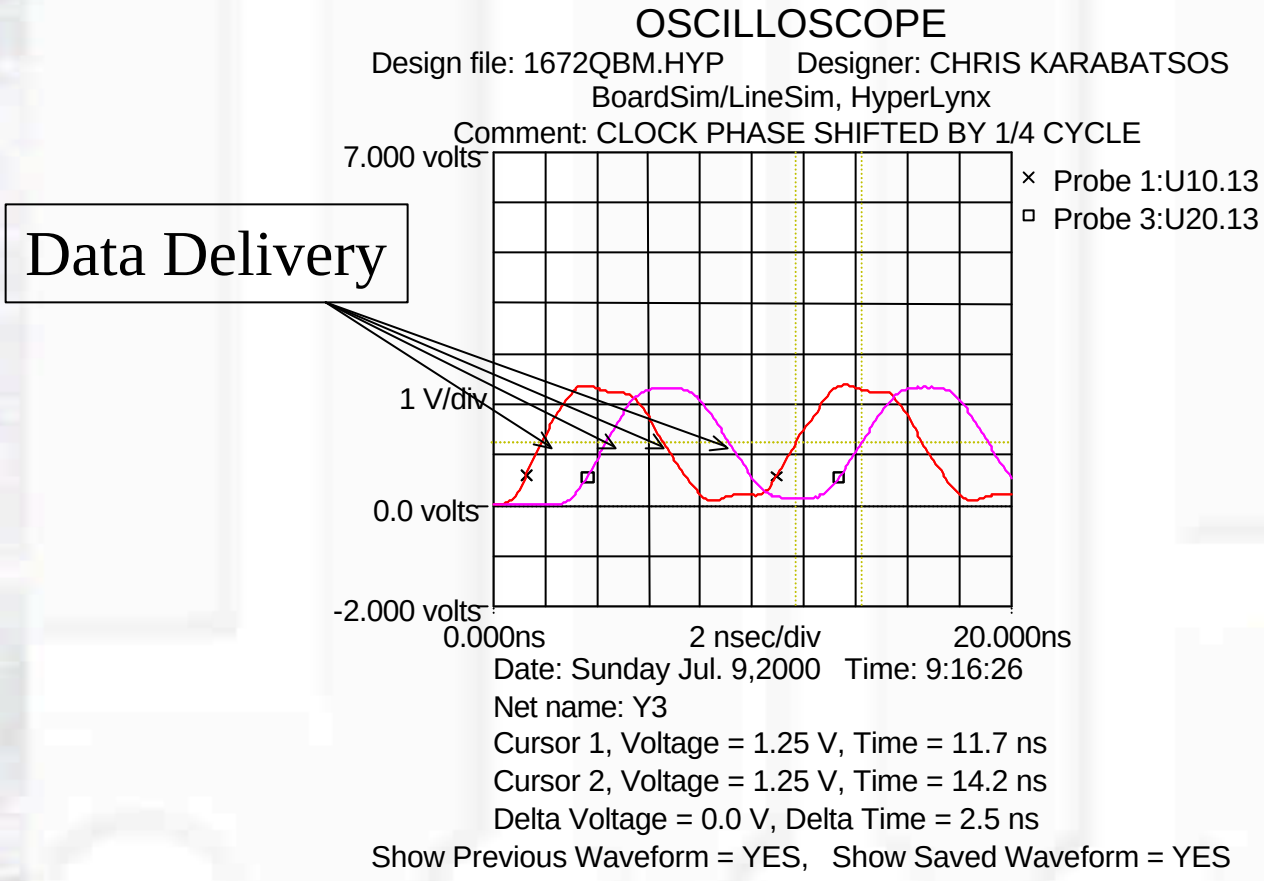
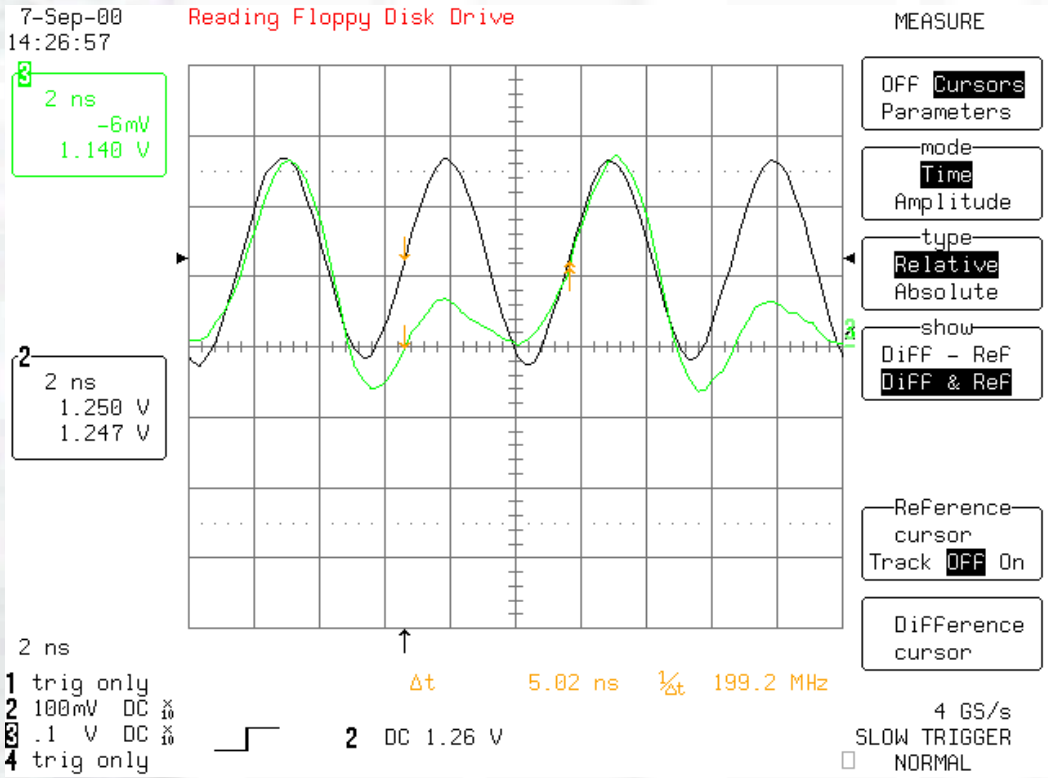
QBM: How does it work?



Actual QBM™ Clock Measurement



- The picture shows actual Clock signal period overlapping the data bit. The signal was taken 5 inches a way with 10 pF and operating at 2.5 Volts.

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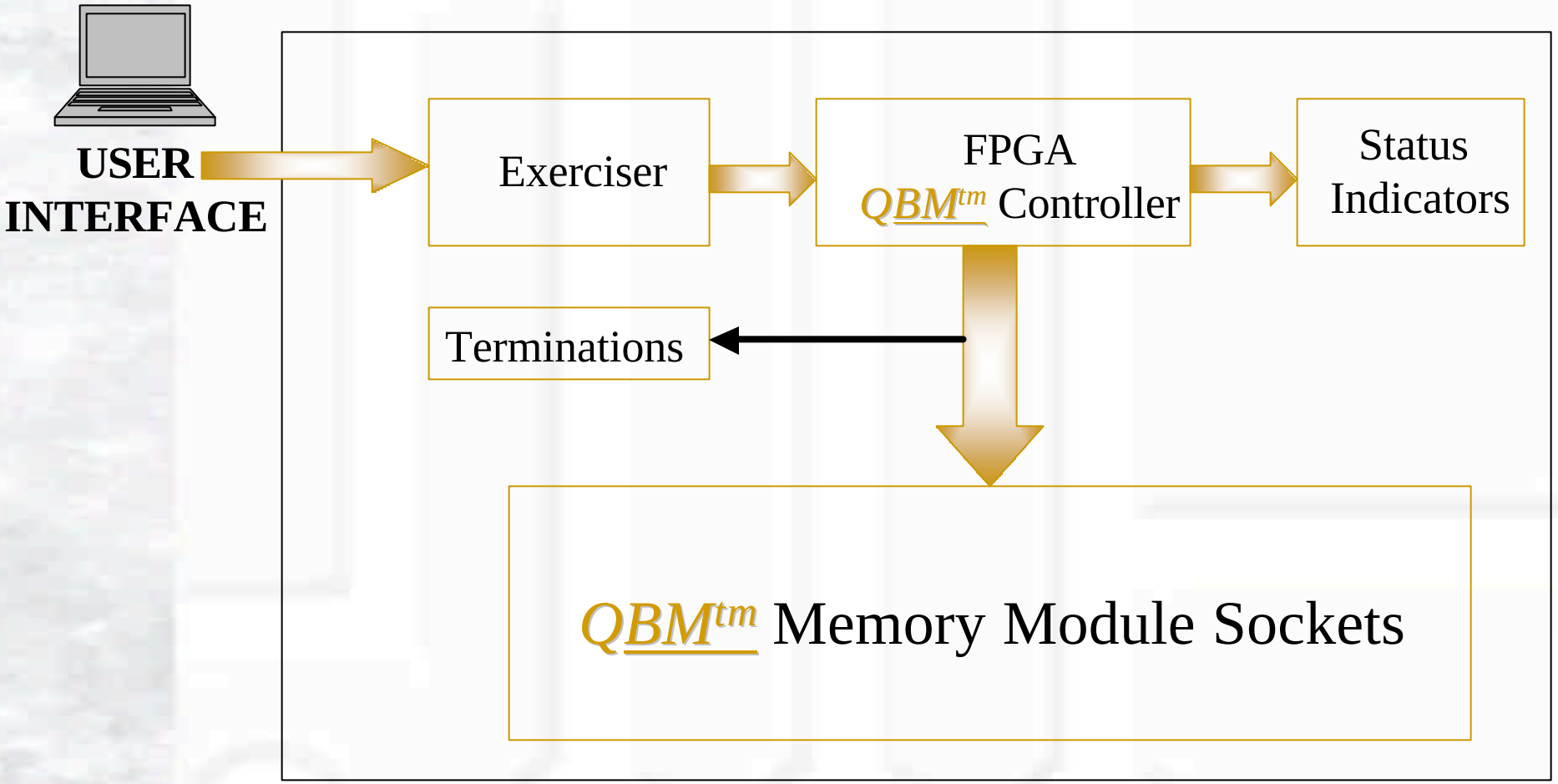
QBM: Program Status

Complete design.	☑ Completed
Internal review.	☑ Completed
Preliminary testing.	☑ Completed
Validation platform	☐ February 2001
Product Characterization	☐ Q1' FY2001
Industry implementation.	☐ 2nd Half FY2001

QBM™ Memory Subsystem



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QBM:Validation Platform

Features:

- It will operate QBM at speed (100MHz clock/400MHz data rate per I/O).
- Memory subsystem will exercise the QBM module in a similar fashion to a system environment.
- A user interface allows to simulate various sets of patterns/timings in a real life system operation.

Benefits:

- Prove the concept of operating DDR SDRAMs in QBM mode.
- Provide with design guidelines for system level integration of QBM high-speed bus interface.
- Preliminary memory controller design that builds the foundation for chipset designers to develop an ASIC controller for QBM.

QBM™
Solutions for Bandwidth

Synchronous DRAM:

Device used:	SDRAM	SDRAM	DDR	DDR (USING QBM™)
Clock speed:	100 MHz	133 MHz	100 / 133 MHz	**100 / 133 MHz**
Data rate:	100 MHz	133 MHz	200 / 266 MHz	**400 / 532 MHz**
Bandwidth:	0.8GB/s	1.03GB/s	1.6/2.1 GB/s	**3.2/4.2 GB/s**
Availability:	Now	Now	Q4-2000	**Q1/2001**
Standard:	PC100	PC133	PC200/PC266	**PC400/PC532**

Sync Flash Memory:

Device used:	SYNC FLASH 100	SYNC FLASH 100 (USING QBM™)
Clock speed:	66/100 MHz	**66/100 MHz**
Data rate:	66/100 MHz	**133/200 MHz**
Bandwidth:	0.5/0.8GB/s	1.02/1.6 GB/s
Availability:	TBD	**Available as soon as Sync Flash 100 is available**
Comments:	Seeking to be identical to PC100	

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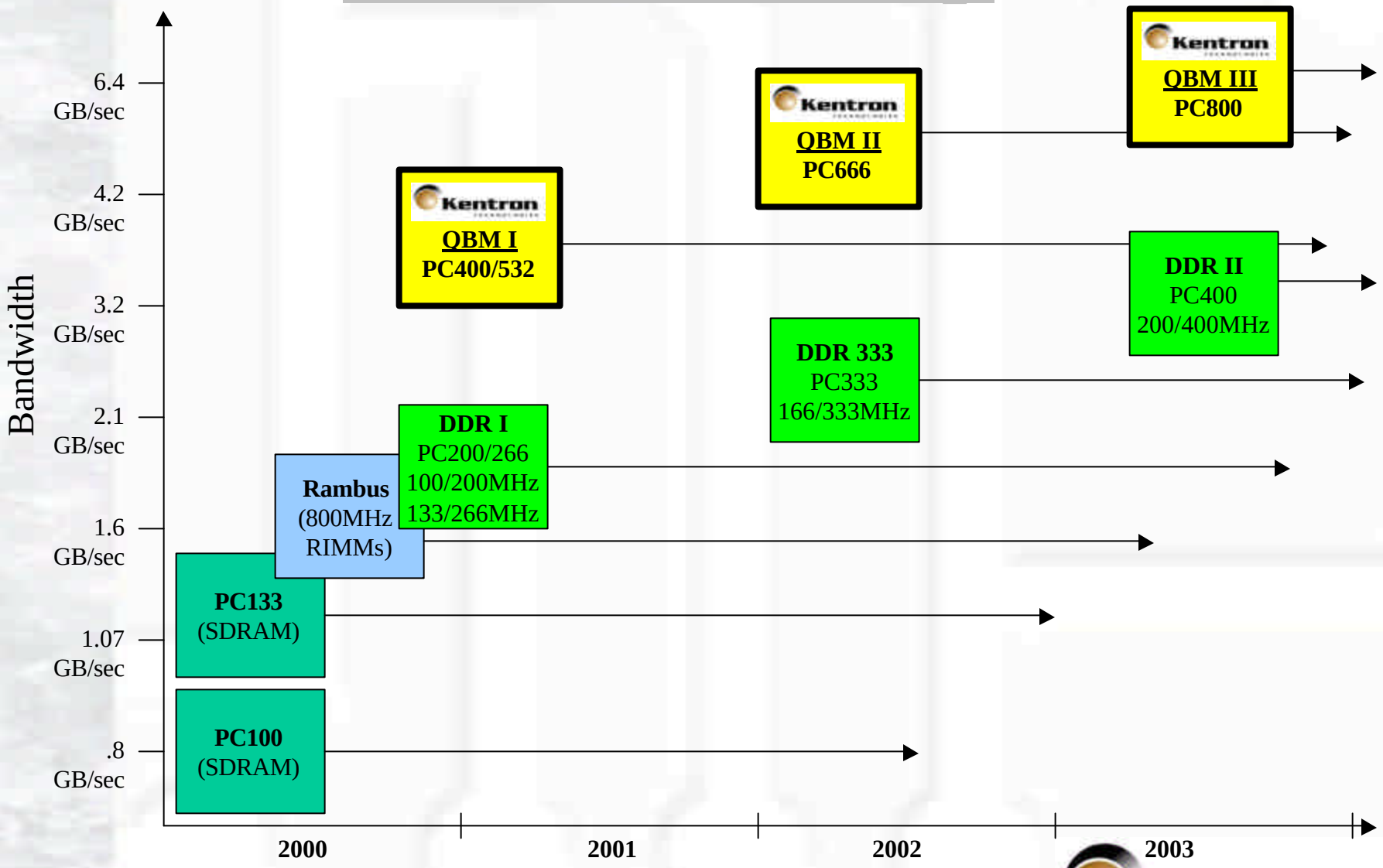
QBM™ Roadmap



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THE PERFECT FIT

64-bit ***QBM™*** *"NARROW BUS" Architecture*

Vs

128-bit DDR "WIDE BUS" Architecture

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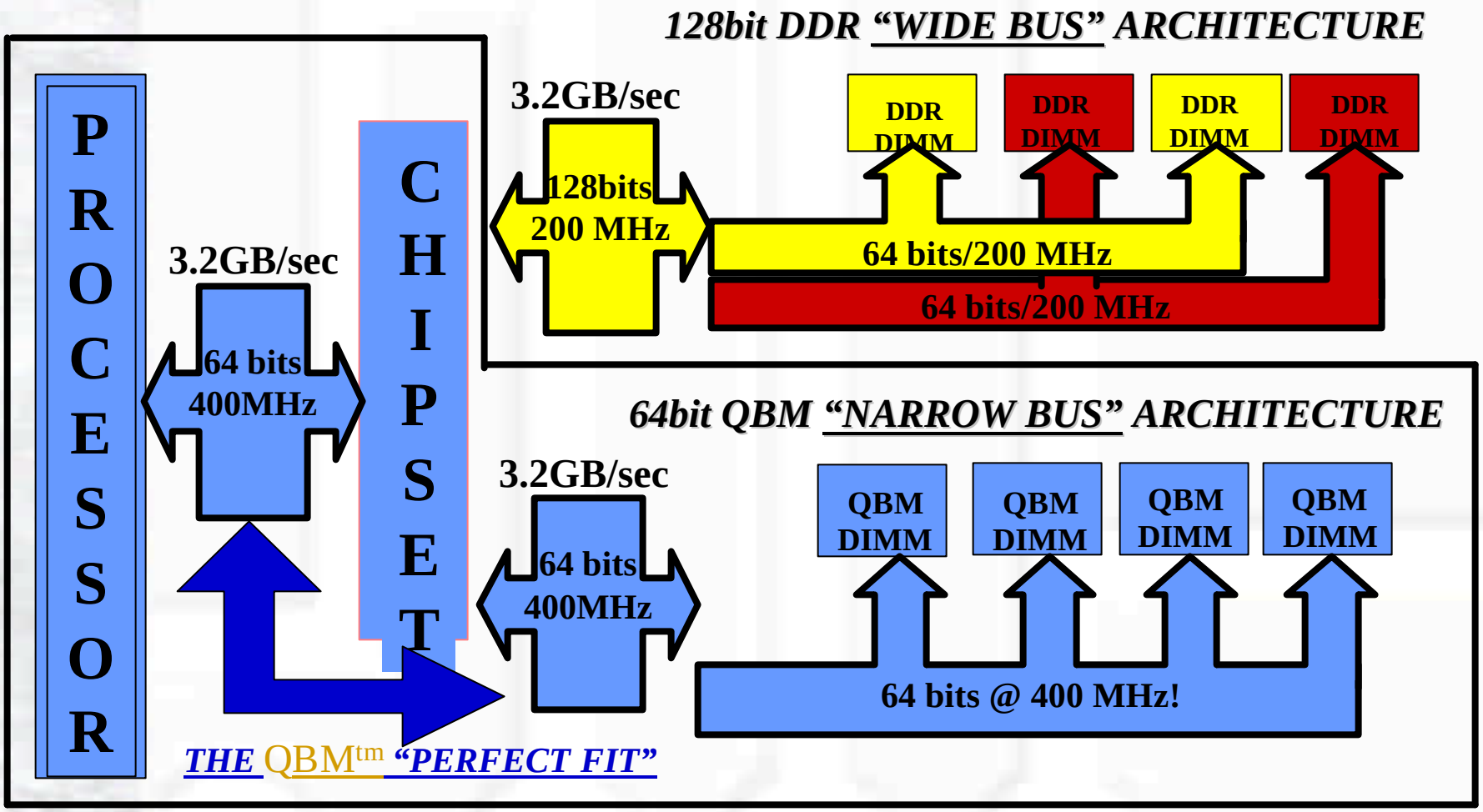
Wider may not be better



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64bit QBM™ "NARROW BUS" Architecture Benefits

- Chipset benefits
- Motherboard benefits
- Upgrade benefits

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Having a 64bit QBM™ "NARROW BUS" Architecture Benefits the Chipset

- ½ Of the number of I/O pins on the chipset (less pins, smaller package, less board space, less cost).
- Simpler chipset core (FIFO, matched speed, no de-mux).
- Chipset input & speed from front side bus (FSB) matches chipset output & speed on the memory bus & vice versa.

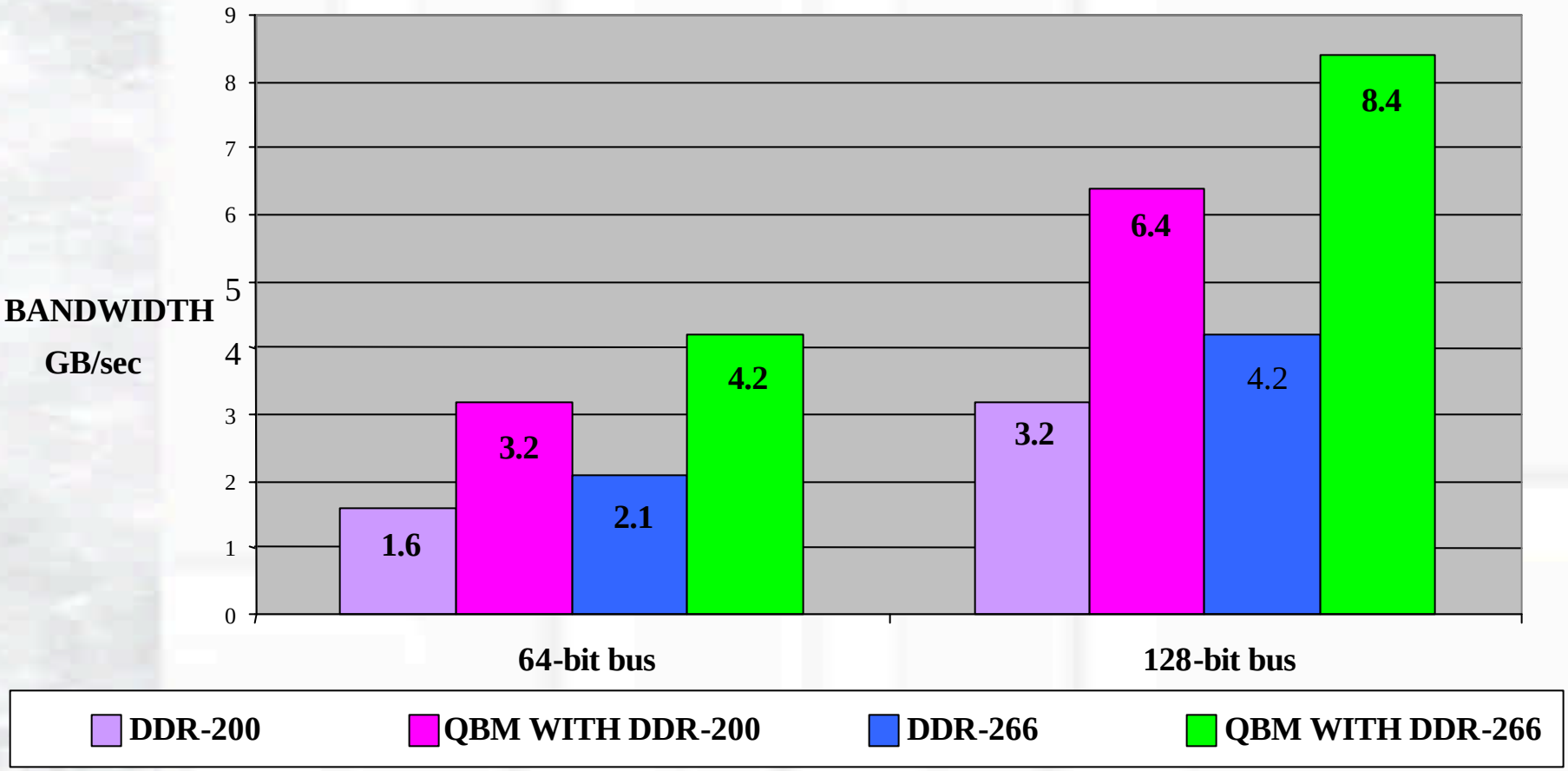
Having a 64bit QBM™ "NARROW BUS" Architecture Benefits the Motherboard

- No change needed to the existing motherboard architecture (existing motherboards are 64bit).
- No extra motherboard layers needed to implement the wiring, therefore no extra costs.
- Data bus width on the motherboard is similar to the memory module width, allowing the system to drive multiple DIMMs (4) with a single data bus.

Having a 64bit QBM™ "NARROW BUS" Architecture Benefits Future Upgrades

- No multiple module granularity (128bit bus requires DIMMs added in pairs versus singular with 64bit).
- Allows mix & match of different memory densities between slots (can not be done with 128bit bus).
- No limitation on upgrading the density in smaller increments (can not be done with 128bit bus).

QBM: Improving DDR Bandwidth



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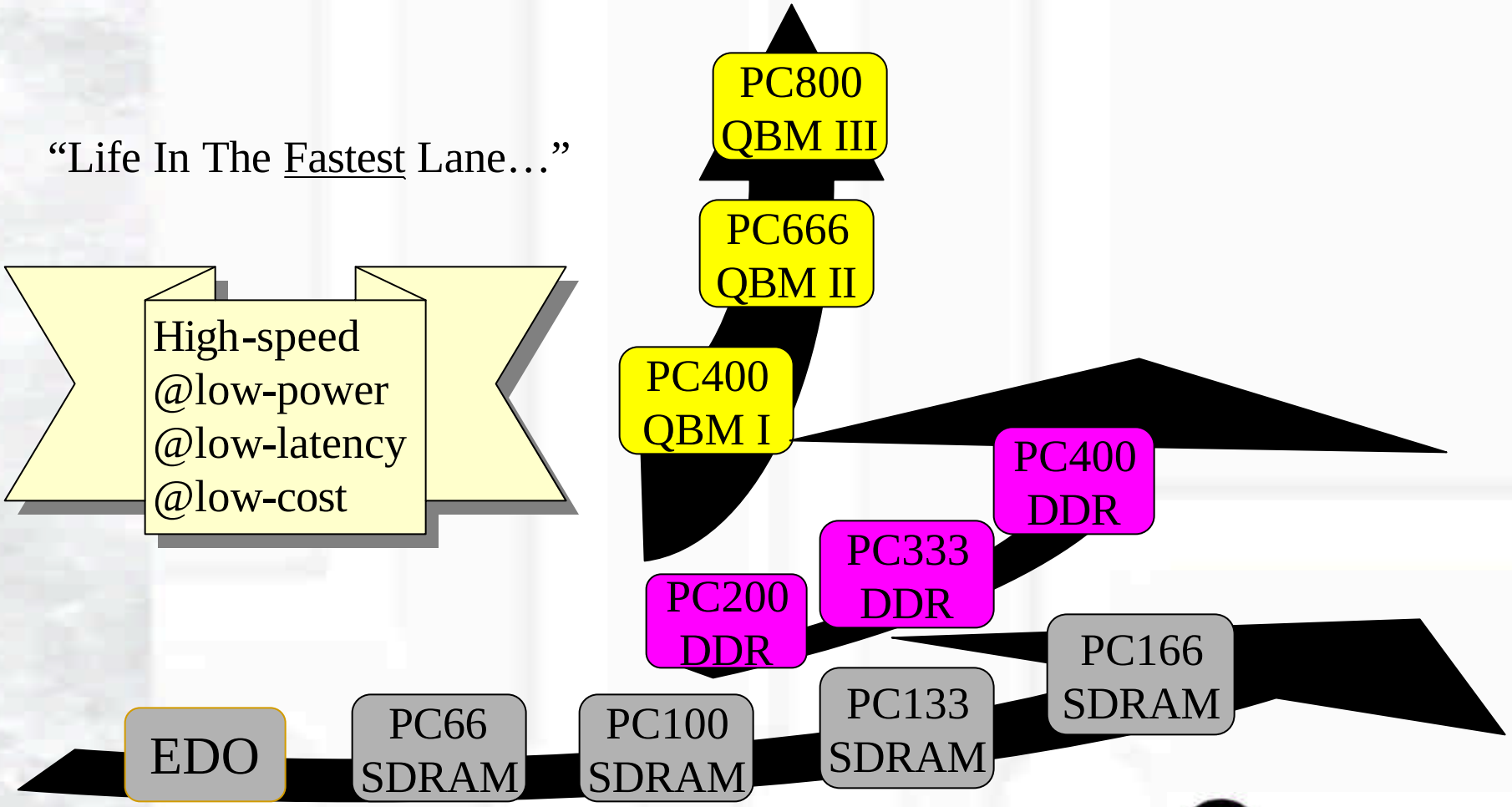
What does all this mean?

- QBM^{tm} is part of a continuous evolutionary path that allows server and telecom platform OEMs to realize dramatic speed improvements ***(3.2/4.2 GB/sec) today***!
- QBM^{tm} maintains industry compatibility and is easily implemented using today's standard "off the shelf" components.
- QBM^{tm} minimizes OEM risk and can be supplied to the industry at a cost-efficient price.
- QBM^{tm} is just in time technology that allows the re-use of the existing industry infrastructure.

QBM™
A Clear Roadmap for the Future



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THE "QBM™ ALLIANCE"

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The Need For Strategic Alliances

Memory Manufacturers

Samsung *Hyundai* *Micron* *Elpida*

Infineon *Mitsubishi* *Mosel-Vitelic* *Toshiba*

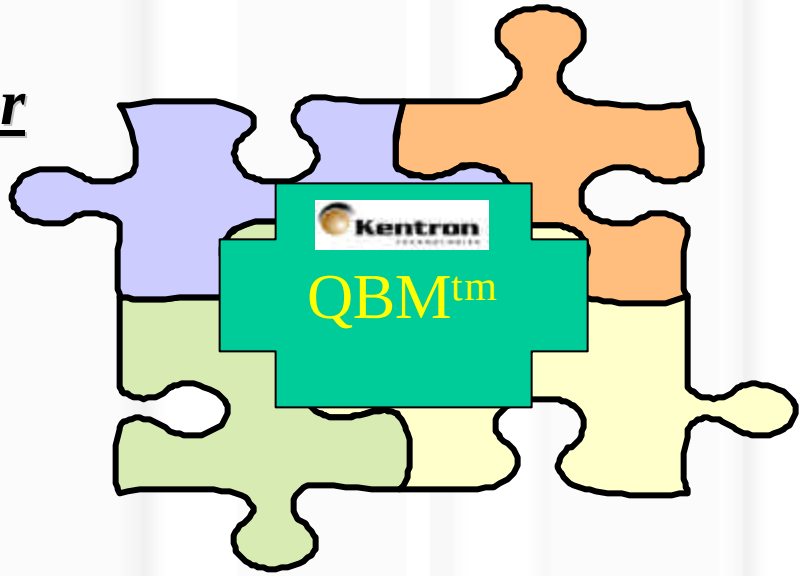
DDR-enabled Chipset/Processor Developers

Intel *AMD*

VIA Tech. *Micron*

SiS *Serverworks*

Sun *Acer Labs.*



Mother Board Manufacturers

Intel *Tyan*

ASUS *Supermicro*

Diamond *Gigabyte*

AMI *Acer*

FIC *A-Bit*

Contract/Module Manufacturers

MCMS *Smart* *Kingston* *PNY* *Celestica* *Wintec*

Crucial *Viking* *Dataram* *Unign* *Advantage* *Corsair*

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Summary
Enabling Platform Technology

- Leading edge (***LOW PROFILE***) platforms for **"1U" environments**.
- Innovative ***(FEMMA)*** solutions for **Memory density** issues.
- Creative ***(E-BUS)*** resolution to **Bus load** challenges.
- Effective ***(QBM)*** approach to enhance **Internet bandwidth**.

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